REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claims 6, 11 and 25 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this rejection.

Claim 6 claims that "the constant voltage is in a range of 3.5 to 6V." The "constant voltage" referred to is the voltage applied to one of the two source/drain regions, as is stated in Claim 1. Paragraph 28 clearly states that "[t]he source region is at ground potential 301 when a voltage in the range of 3.0 to 6V is applied to the drain region 305." The claimed range of 3.5 to 6V is clearly in the range of 3.0 to 6V as discussed in the specification.

Claim 11 claims that "the constant voltage is in a range of 3.5 to 6V and the ramp voltage starts in a range of 0 to 6V and ends in a range of 4 to 12V over a time period in a range of 1 microsecond to 1 millisecond." Again, the constant voltage as claimed by claim 1 is the voltage applied to one of the two source/drain regions. As shown in the previous paragraph, paragraph 22 teaches the range of 3.5 to 6V. Paragraph 29 states that "[a] linear ramp voltage is applied to the control gate of the cell 307. In one embodiment, this voltage starts in the range of 0 to 6V and goes up to 4 to 12V for a time in the range of 0.001 – 1 millisecond." It is well know by one skilled in the art that the 0.001 millisecond in the specification is the same as the 1 microsecond as claimed in claim 11.

Claim 25 has a typographical error that has been corrected above. The first negative voltage range should end at –4V and the second negative voltage range begins at –7V as indicated by only one of the embodiments of the present invention.

Claims 1-2, 12, 18, 21, 24 and 26-27 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection.

MPEP 2703.05(e) states in pertinent part:

> Obviously, however, the failure to provide explicit antecedent basis for terms does not always render a claim indefinite. If the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter.

1992) ("controlled stream of fluid" provided reasonable antecedent basis for "the controlled fluid"). Inherent components of elements recited have antecedent basis in the recitation of the components themselves. For example, the limitation "the outer surface of said sphere" would not require an antecedent recitation that the sphere has an outer surface.

The claims in question recite "two source/drain regions". If a voltage is applied to one of those source/drain regions, "the remaining" source/drain region is inherent in the "two source/drain regions". It is inherently obvious that there can only be one "remaining" source/drain region since one of two is already used. Therefore, as provided in the above-cited MPEP section, the scope of the claims in question would be "reasonably ascertainable by those skilled in the art."

Allowable Subject Matter

Claims 1, 12, 18, 21 24 and 26-27 were rejected under 35 U.S.C. 112, 2nd paragraph, but would be allowable if rewritten or amended to overcome these rejection(s).

Claims 2, 6, 11 and 25 were rejected under 35 U.S.C. 112, 2nd paragraph, but would be allowable if rewritten to overcome these rejections, including all of the limitations of the base claim and any intervening claims.

Claims 3-5, 7-10, 13-17, 19-20 and 22-23 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

CONCLUSION

For the foregoing reasons, Applicant believes the present invention is in condition for allowance. Therefore, Applicant respectfully requests withdrawal of the rejection and allowance of claims 1 – 27. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No additional matter has been entered and no additional fee is required by this amendment and response.

Respectfully submitted,

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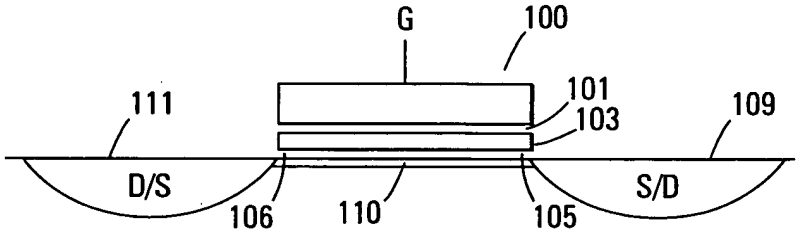

Fig. 1A

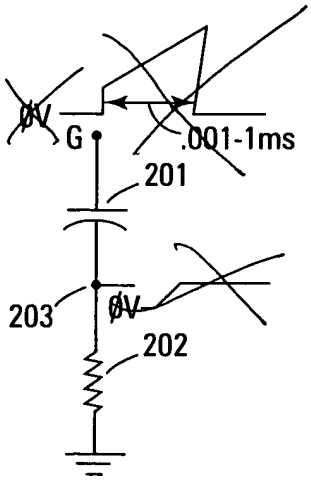

Fig. 2

AMENDMENTS TO THE DRAWINGS

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they included the following reference character(s) not mentioned in the description: 0V and .001-1ms in Fig. 2; CONTROL, DATA, and ADDRESS in Fig. 6. Applicant respectfully traverses this objection.

The labels "0V" and ".001-1ms" are discussed in the specification at paragraph 29 where it states that "[a] linear ramp voltage is applied to the control gate of the cell 307. In one embodiment, this voltage starts in the range of 0 to 6V and goes up to 4 to 12V for a time in the range of 0.001 – 1 millisecond." Since the circuit of Fig. 2 is the equivalent circuit of the NROM cell of Fig. 1 and the gate connection "G" is clearly labeled in both figures, it is clear that the ramped voltage of Fig. 2 with the labels "0V" and ".001-1ms" is being applied to the gate connection as is referred to by paragraph 29. However, in the interest of expediency, Applicant has deleted these references from Fig. 2.

The labels "CONTROL", "DATA", and "ADDRESS" are shown in Figure 6 as being coupled to a microprocessor. 37 CFR 1.84(n) states that "[g]raphical drawing symbols may be used for conventional elements when appropriate. The elements for which such symbols and labeled representations are used must be adequately identified in the specification. Known devices should be illustrated by symbols which have a universally recognized conventional meaning and are generally accepted in the art." It is well known by one skilled in the art that a microprocessor generates a control bus, a data bus, and an address bus. Therefore, the microprocessor with its control, data, and address bus is a symbol that is well known in the art and not in need of further discussion. However, again in the interest of expediency, Applicant has amended the specification at paragraph 38 to add these labels.

The drawings were objected to as failing to comply with 37 CFR 1.83(a). The Examiner stated that the two source/drain regions and an NROM cell embedded in a CMOS device must be shown or canceled from the claims. Applicant respectfully traverses this objection.

The two source/drain regions are clearly shown in both Figure 1A and 1B as reference numbers 109 and 111. In order to fit the labels "source/drain" into the small areas, these terms had to be abbreviated "D/S" and "S/D". These areas are clearly described as source and drain at paragraph 22 of the specification. While the phrase "drain/source" is not explicitly used in the specification, it is well known by those skilled in the art that only one area (109 or 111) is a drain and the other area (111 or 109) a source at any one time. Paragraph 22 clearly states that the

source and drain functions change with the direction of operation of the cell. Therefore, while one area 111 is a drain (i.e., D), the other area 109 is a source (i.e., S), hence the D/S label. Similarly, when the first area 111 is a source, the other area 109 is a drain, hence the S/D label. Therefore, the two source/drain and drain/source regions that are recited in the claims are clearly discussed in the specification and shown in the drawings.

Applicant has amended paragraph 38 to include the term "CMOS". This type of system has been mentioned many times throughout the specification so no new matter has been added.